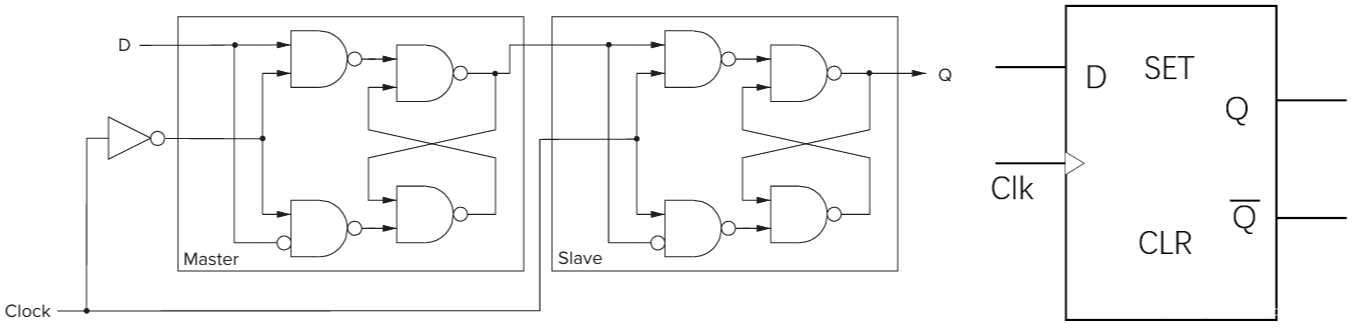
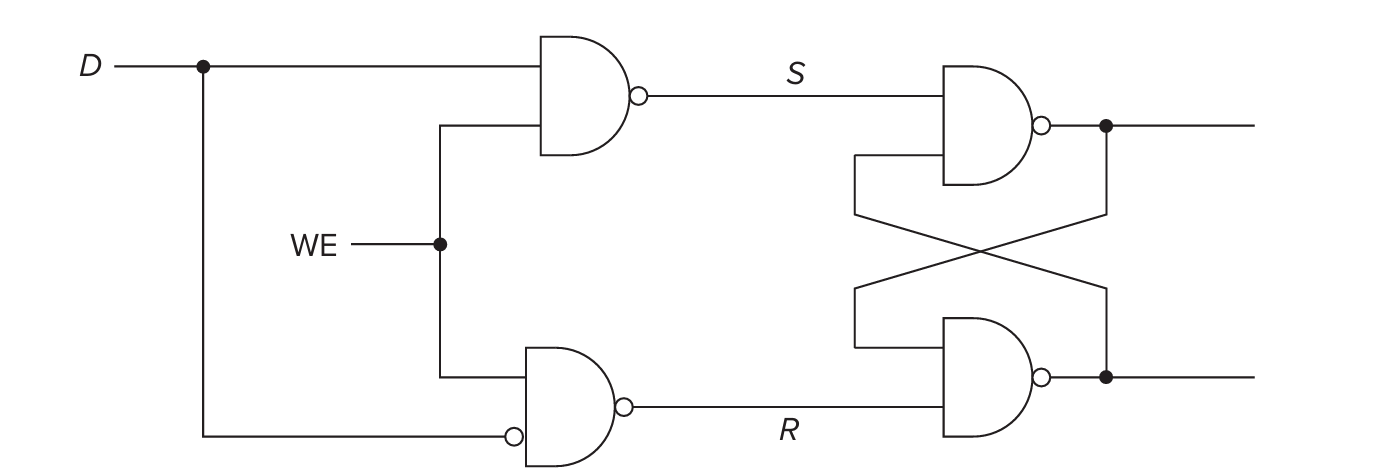
锁存器 / 触发器

* R-S Latch
  + 注意与非门版本和或非门版本的区别
  + 与非门：低电平触发；或非门：高电平触发
  + 与信号位置相反
* Gated D Latch
  + 时，输出保持不变
  + 时，输出跟随变化
* Master/Slave Flip-flop(D Flip-flop)
  + 当且仅当**由变为（时钟周期开始）**时，  
    输出随变化

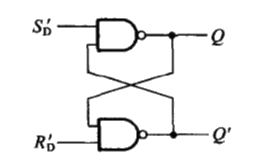
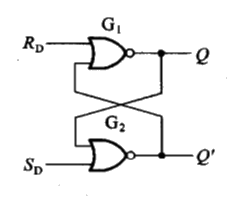


D Flip-flop

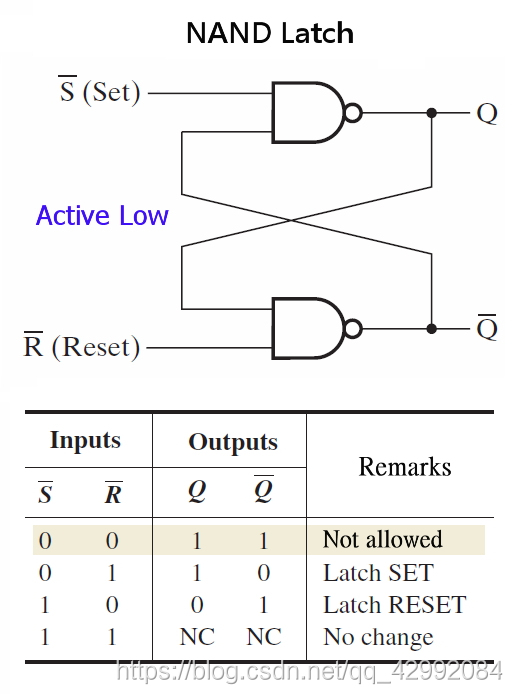
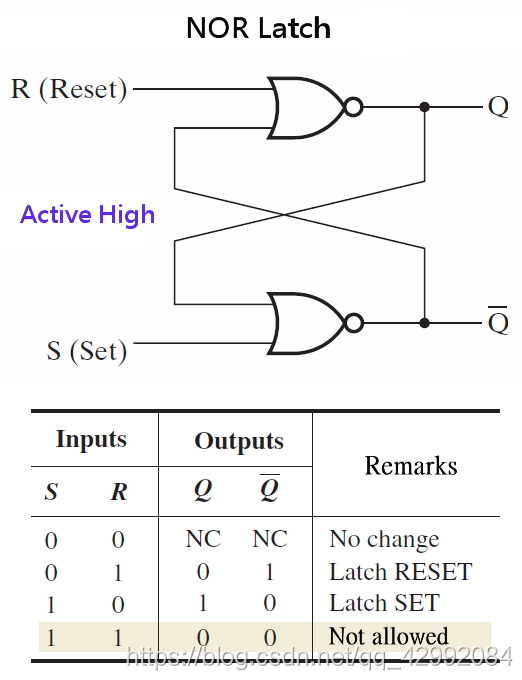


Gated D Latch

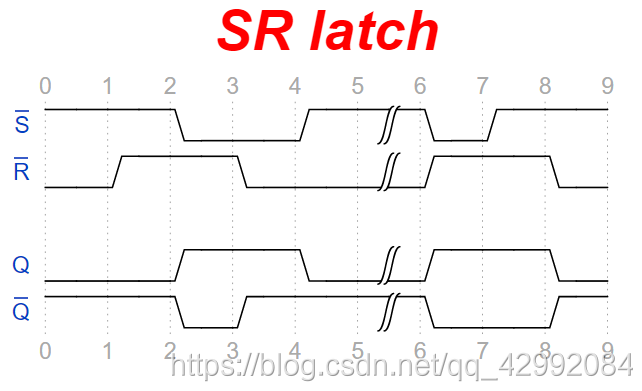
R-S Latch



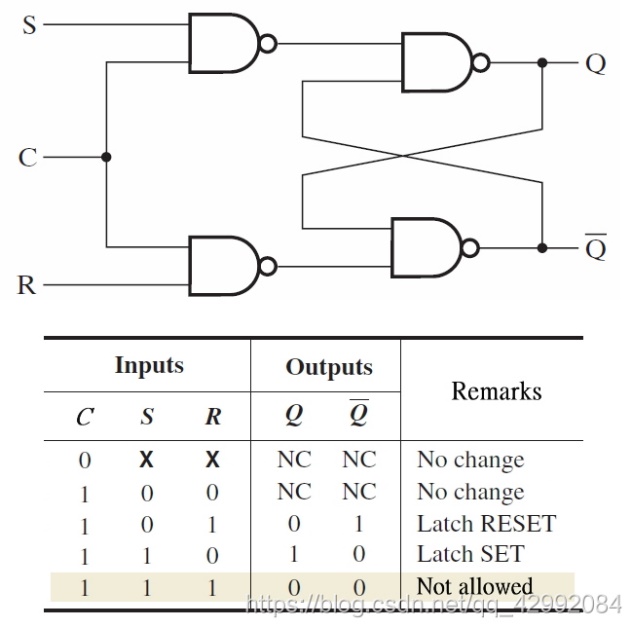
R-S锁存器



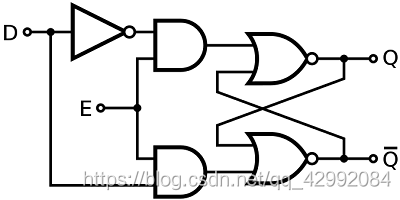
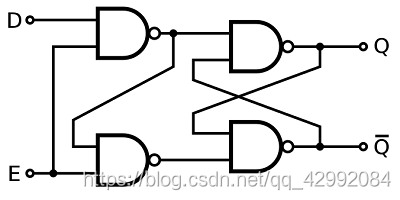
NAND为例：时序分析



门控R-S锁存器

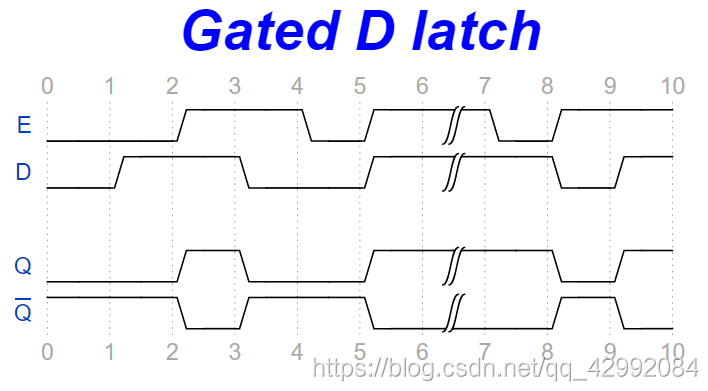


门控D锁存器

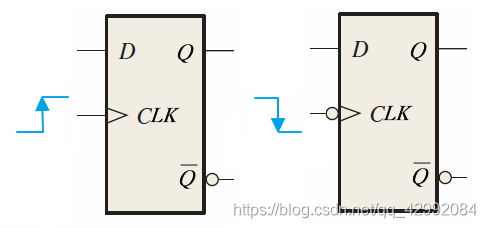


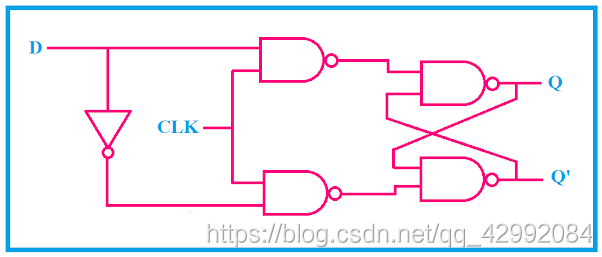
左：基于NAND 右：基于NOR

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| E | D | Q | Q— | Comment |
| 0 | X | Qprev | Q—prev | No change |
| 1 | 0 | 0 | 1 | Reset |
| 1 | 1 | 1 | 0 | Set |

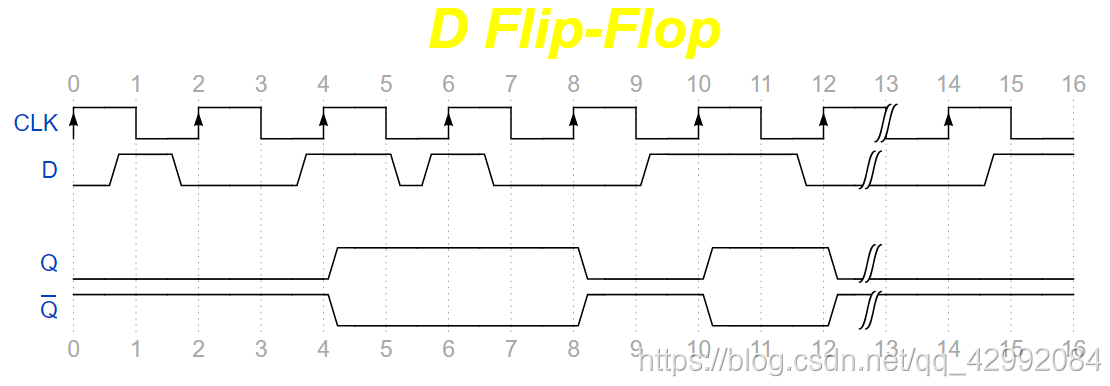
时序分析  


D触发器





|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| 触发 | D | Q | Qnext | Comment |
| ↘ | X | Qprev | Q | No change |
| ↗ | 0 | 0 | 0 | Reset |
| ↗ | 0 | 1 | 0 | Reset |
| ↗ | 1 | 0 | 1 | Set |
| ↗ | 1 | 1 | 1 | Set |



逻辑完备

NAND 逻辑完备

NOT (A) = NAND (A, 1)

AND (A, B) = NAND (NAND (A, B), 1)

OR (A, B) = NAND (NAND (A, 1), NAND (B, 1))

NOR 逻辑完备

NOT (A) = NOR (A, 0)

OR (A, B) = NOR (NOR (A, B), 0)

AND (A, B) = NOR (NOR ((A, 0), 0), NOR ((B, 0), 0))

XAND 逻辑不完备  
XOR 逻辑不完备

